REMARKS/ARGUMENTS

Prior to entry of this Amendment, claims 1-64 were pending in the above referenced application.

Claims 1-64 have been rejected under 35 U.S.C. § 251. According to the Examiner, original patent (U.S. Patent No. 6,021,265) expired for failure to pay a maintenance fee.

Additionally, claims 1-64 have been rejected under 35 U.S.C. § 103 as obvious over U.S. Patent No. 5,542,059 to Blomgren ("Blomgren I") in view of U.S. Patent No. 5,781,750 to Blomgren et al. ("Blomgren II").

Pursuant to this Amendment, new claims 65-70 are now pending in the application. No new matter has been added.

I. Rejections Under 35 U.S.C. § 251

Claims 1-64 have been rejected under 35 U.S.C. § 251 based upon the Examiner's contention that original patent (U.S. Patent No. 6,021,265) expired for failure to pay a maintenance fee. The basis for this rejection is factually incorrect. All maintenance fees for the original patent have been timely paid; the original patent has never expired. Copies of internet web pages from the U.S. Patent and Trademark Office (Finance Office) establishing conclusively that the maintenance fees have been paid, are attached as a courtesy. The rejection under 35 U.S.C. § 251 should be withdrawn.

II. Rejections Under 35 U.S.C. § 103(a)

Claims 1-64 have been rejected under 35 U.S.C. § 103(a) as allegedly obvious over Blomgren I in view of Blomgren II.

A *prima facia* case of obviousness has not been established with respect to any of the pending claims. The combination of Blomgren I and Blomgren II, whether taken alone or in combination, does not disclose all of the limitations of any pending claims, as required to support rejection under 35 U.S.C. § 103(a).

A *prima facie* case of obviousness requires each of the following three requirements to be met:

1. the cited prior art references must teach or suggest all the claim limitations;
2. there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine the references' teachings; and
3. there must be a reasonable expectation of success.

In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Additionally, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on Applicant's disclosure. *Id.* Absent evidence that each of the above three requirements are met, a rejection under 35 U.S.C. § 103(a) is improper.

There has been no showing that the cited prior art references, whether alone or in combination, teach or suggest all the claim limitations of any claim. The rejections under 35 U.S.C. §103(a) are without merit and should be withdrawn.

A. **Claims 1-14**

Claim 1 (and claims 2-14 which depend from it) have been rejected based on a contention that Blomgren I (citing col. 8, lines 41-43 and Fig. 4) and Blomgren II disclose a program counter register. Neither of these describes or discloses a program counter register. In fact, the cited passage of Blomgren I apparently relates to an instruction fetcher and provides no details

on what the instruction fetcher contains. Even assuming, without conceding, that Blomgren II discloses an instruction pointer, it does not disclose or suggest that "one or more predetermined indicator bits of said program counter [are] operable to control said processor core to execute program instruction words of a current instruction set selected from said predetermined plurality of instruction sets and specified by the state of said one or more indicator bits of said program counter register" as required by claim 1 and by claims 2-14 that depend from it.

The rejection also relies improperly upon the Applicant's disclosure in the '265 patent for the recognition that unused bits in a program counter register may be used to indicate the current instruction set. This, though, is neither disclosed nor suggested by Blomgren I or Blomgren II or elsewhere in the art but relies on impermissible hindsight to reconstruct Applicant's invention as described in claim 1. *In re Dembiczak*, 175 F.3d 994, 999 (Fed. Cir. 1999) (obviousness analysis may not use hindsight with the benefit of applicant's disclosure), *overruled on other grounds, In re Gartside*, 203 F.3d 1305, 1316 & 1319 (Fed. Cir. 1999) (retaining prohibition on hindsight based obviousness analysis); *ATD, Corp.* v. *Lydall, Inc.*, 159 F.3d 534, 546 (Fed. Cir. 1998) (improper to use hindsight to cull selected elements from prior art). For this reason alone, the rejection of claims 1-14 as obvious should be withdrawn.

Further, both Blomgren references refer to CISC instructions, which are generally not of a fixed length. When CISC instructions of varying length are stored in memory, there are no clear and predictable boundaries between instructions such that one could predict that certain bits in the program counter register, such as the least significant bits, would not be needed. Accordingly, it would appear that Blomgren I and Blomgren II could not necessarily be modified in a manner that would meet the limitations of claim 1. Blomgren I and Blomgren II do not disclose the use of a program counter register to contain an indicator bit. There is no reason to

believe that, if these references used a program counter register, that they would lead to a memory access controller that is not responsive to one or more predetermined indicator bits of the program counter register, as also required by claim 1 and its dependencies. For these reasons, claim 1, and claims 2-14 that depend from it, recite allowable subject matter.

Further, with respect to claims 3-6, neither Blomgren reference discloses two instruction sets that contain instructions of fixed length, such as X-bits (or 32 bits) and Y-bits (or 16 bits). At least one of the instruction sets referenced in Blomgren I and Blomgren II is a CISC instruction set, which may contain instructions of varying length, not fixed length instructions as reflected in claims 3-6.

The remaining rejections with respect to claims 7-14 are also misplaced. Neither Blomgren I nor Blomgren II discloses using bits of a program counter register as an instruction set indicator, much less using particular bits in the program counter register for this purpose.

For all of the foregoing reasons, the rejection of claims 1-14 under 35 U.S.C. § 103(a) should be withdrawn.

B. **Claims 15-64**

Blomgren I and Blomgren II, whether taken alone or in combination, neither disclose nor suggest that a sequence of bits accessed in response to an instruction contains both an address portion and an instruction set indicator portion as recited in method claims 15, 21 and 57 as well as all claims that depend from them. Similarly, apparatus claims 27, 33, 39, 45 and 51 (and all claims dependent thereon) contain a limitation concerning the processor core accessing a sequence of bits in response to an instruction where the sequence of bits contains both an address portion and an instruction set indicator portion. Among other limitations that are missing, neither Blomgren I nor Blomgren II, whether alone or in combination, discloses, teaches or suggests a

method or apparatus containing such limitation. In fact, neither Blomgren I nor Blomgren II describe how a mode control circuit is set, much less a sequence of bits containing both an instruction address and an instruction set indicator portion.

The Examiner references col. 9, lines 60 – col. 10, line 14 and Figs. 4 and 5 of Blomgren I. Neither Blomgren I nor Blomgren II provide any information concerning the method by which a mode control circuit determines whether an instruction is a CISC instruction or a RISC instruction; nor do they describe a sequence of bits that contains both an address portion and an instruction set indicator portion. There is simply no basis in the disclosure of either reference to conclude that the "current instruction set for the data processing apparatus is the instruction set identified based on the instruction set indicator portion of the sequence of bits." The only way to arrive at the conclusion as necessary to sustain the rejection is via impermissible hindsight using the teachings of the present application to read into the disclosure of the Blomgren references something that is not described therein. *In re Dembiczak*, 175 F.3d 994, 999 (Fed. Cir. 1999) (obviousness analysis may not use hindsight with the benefit of applicant's disclosure), *overruled on other grounds, In re Gartside*, 203 F.3d 1305, 1316,1319 (Fed. Cir. 1999) (retaining prohibition on hindsight based obviousness analysis); *ATD, Corp.* v. *Lydall, Inc.*, 159 F.3d 534, 546 (Fed. Cir. 1998) (improper to use hindsight to cull selected elements from prior art). Accordingly, the rejection under 35 U.S.C. § 103(a) is traversed because it has not established a *prima facie* case of obviousness. *See In re Fritch*, 972 F.2d 1260, 1265, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992).

With respect to pending claims 28, 31, 32, 34, 37, 38, 40, 43, 44, 46, 48, 49, 50, 55, 56, 59 and 60-64 (and claims that depend from them) and new claim 65, it is also clear that neither Blomgren reference teaches, discloses or suggests that the circuit used to indicate the instruction

set is included as part of a program counter register. For purposes of clarity, Applicant notes that in a pipelined processor there may be more than one physical program counter, including for example a program counter register associated with each of the pipeline stages. The Examiner's contention that it is well known that bits of a program counter are unused (and thus necessarily available for use in Applicant's invention) is misplaced in the context of the Blomgren references: those references involve the use of CISC instructions of varying length. Since the instructions in a CISC instruction set often vary in length, the instruction boundaries in memory do not necessarily occur on clear, predictable boundaries and it would be inappropriate to assume that a portion of the program counter in the Blomgren references remained available for use as an instruction set indicator. For this same reason, the Blomgren references do not disclose instruction sets of X-bit and Y-bit instructions since the CISC instructions would vary in length. Accordingly, the Blomgren references do not disclose the concept of using otherwise unused bits in the program counter register to identify the current instruction set nor do they disclose the concept of using a single instruction to access a sequence of bits that specifies both the address of an instruction and the instruction set to which the instruction belongs.

C. **Conclusion**

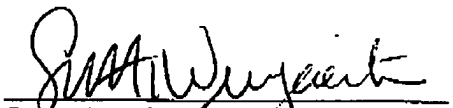
Since each of the pending claims recite subject matter that is neither taught nor suggested by the art of record, none of the pending claims are *prima facie* obvious. Accordingly, the Applicant requests that the rejections under 35 U.S.C. § 103(a) be withdrawn.

III. CONCLUSION

Upon entry of this Amendment, **claims 1-70** are pending in the application. Applicants submit that the claims, for the reasons set forth above, are now in condition for allowance. Reconsideration and allowance are therefore respectfully requested.

Dated: 12/17/04

Respectfully submitted,



Scott T. Weingaertner
Reg. No. 37,756
Attorney for Applicant

Customer No. 07470
Attorney's Direct Line: (212) 819-8404